

APR 22 2008

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**OPERATOR:** Janice S**TIME COMPLETED:** \_\_\_\_\_**EXT. NO.:** 524**DATE:** April 22, 2008**OUR FILE NO.:** 411000-138

<b>NAME</b>	<b>FIRM:</b>	<b>FAX NO.</b>
Swapneel Chhaya	U.S. PTO	1-571-270-2434

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**FROM:** William Squire      **Total Pages Including Transmittal Sheet:** 3

**COMMENTS:** \_\_\_\_\_

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APR 22 2008

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Walter Fix et al.

Serial No.: 10/541,957 Filed: Feb. 2, 2006

Title: ORGANIC FIELD EFFECT TRANSISTOR AND INTEGRATED CIRCUIT

Examiner: Swapneel Chhaya Art Unit: 2822

Atty. Dkt: 411000-138 Customer No. 27162

**PROPOSED AMENDED CLAIM 1 UNDER 37 CFR 1.116**

VIA FAX 571 270 2434  
Commissioner for Patents  
Box 1450  
Alexandria, VA 22313-1450

Sir:

This paper is in view of an examiner's telephone interview with the undersigned on April 22, 2008 and who proposed the below amended claim 1 that is believed to overcome the cited reference rejection over Hart as discussed in the interview. Hart does not show or suggest the limited overlap or the problem overcome as claimed, calling for:

wherein the second electrode layer completely overlies the current channel and overlies a portion of the source or drain electrodes of the first electrode layer, the overlying portion with respect to the source or drain electrodes having a width solely in the range from about 0 to about 20  $\mu$ m

Hart does not recognize that limiting the overlap as claimed will minimize parasitic capacitance as claimed. Hart's overlap is many orders of magnitude greater. See applicants' spec. page 4, lines 15-26, discussing this. Hart does not recognize the problem with parasitic capacitance or its cause. One of ordinary skill is given no direction or hint by Hart of this problem or the claimed solution. The parasitic capacitance term is a whereby clause that results from the claimed structure and thus is